Simulation and Measurement of Quasi-Optical Multipliers

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***Abstract*—The lumped-element finite-difference time-domain method is used to analyze quasi-optical multipliers based on diode loaded slot antennas. The method is validated firstly for a passive microstrip-fed structure then for the diode loaded case in both small- and large-signal regimes. The diode model is separately validated using a series diode mounted on a microstrip line. Input return loss and radiation patterns show good agreement with measurements and the concept of effective conversion loss is introduced and results show reasonable agreement between measurement and simulation. A new diode arrangement is introduced where dual offset diodes are placed in the slot instead of the conventional central diode. The diode position can then act as an extra design parameter. The performance of the two structures has been compared; currently best performance is still obtained for the central-diode structure. Finally, a fully quasi-optical structure is simulated with plane-wave excitation. Central and dual-diode structures are again compared and the diode position and input plane-wave field strengths are optimized. Slot voltage distributions, radiation patterns, and effective quasi-optical conversion losses are presented.**

***Index Terms*—CAD, FDTD, multipliers, quasi-optics, slot antennas.**

I. Introduction

QUASI-OPTICAL circuits that embed active devices within radiating structures are becoming increasing popular in the millimeter and sub-millimeter bands due to their advantages of free-space combining, reduced transmission loss, and multifunctionality [1]. To realize optimum designs for these circuits, it is essential to simulate the entire circuit, both active and radiating parts concurrently. A promising method for achieving this is the lumped-element (LE) finite-difference time-domain (FDTD) method [2], [3]. This approach allows for the incorporation of lumped element models including passive, active, and nonlinear devices directly into the traditional FDTD grid structure [4], [5]. This paper aims to validate this approach and illustrate that it is an accurate and flexible design tool for quasi-optical circuits.

This study is being carried as part of a consortium working on sub-millimeter wave quasi-optical multipliers, in particular, a 150–300-GHz doubler [6]. A working doubler has been fabricated on silicon, however, the structure requires further optimization. This paper presents results for scaled frequency models operating below 20 GHz, which have been used to validate the method and further the understanding of important issues relating to LE-FDTD simulation of these types of circuits.

The quasi-optical multiplier being investigated is based on a Schottky barrier diode mounted in a slot antenna. Slot antennas have been widely used in a number of quasi-optical components for over two decades; these include mixers [7], multipliers [8], and oscillators [9]. The slot antenna possesses a number of features that lends itself to use in quasi-optical systems. Its uniplanar nature facilitates simple mounting of active devices without the need for ground via connections. Also, since only one layer of metallization is required, the antenna can be mounted directly onto the surface of a dielectric lens [10], [11].

This paper begins by presenting a comparison of measured and simulated results for a passive microstrip-line-fed slot-antenna structure, including input return loss and radiation patterns.

The following section describes the validation of the diode model being used within the FDTD grid. The diode is a Hewlett-Packard HSMS-8202, which is a dual-diode package; however, only one of the diodes is being used, the other is left open circuit. All the parasitics of the package are included and the model elements are tuned to account for nonideal behavior of the lumped elements within the LE-FDTD implementation. The diode is simulated and measured connected in series with a 50-Ω microstrip line.

The diode model is then combined with the passive slot antenna structure and small-signal results are presented for input return loss and radiation patterns. The circuit used is unbiased since, although improved performance can be obtained for multipliers with the use of bias, it is felt in large-array environments, the increase in design complexity would outweigh these advantages. The flexibility of the LE-FDTD method is shown by altering the conventional diode position: central in the slot to two offset diodes placed near the ends of the slot. By introducing this extra degree of freedom, it may be possible to obtain improved conversion efficiency over conventional multipliers.

The structure is then simulated and measured in the large-signal regime and input return loss and radiation patterns are again presented. Since this is now large signal, multiplier behavior is observed and both fundamental and first harmonic radiation patterns are shown. A figure-of-merit known as effective

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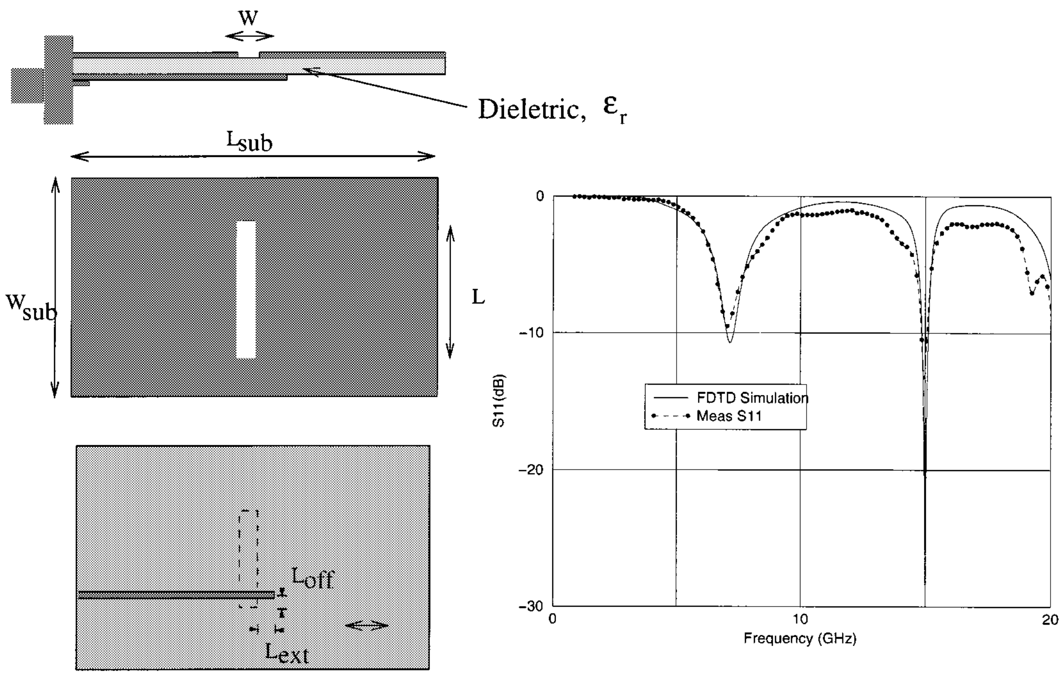


(a) (b)

Fig. 1. (a) Microstrip-fed slot antenna, $L_s = 15.1$ mm, $W_s = 0.4$ mm, $L_{\rm ext} = 4.35$ mm, $L_{\rm off} = 1.5$ mm, $h = 0.813$ mm, $L_{\rm sub} = 25$ mm, $W_{\rm sub} = 23.5$ mm, and $\epsilon_r = 3.38$. (b) Measured and simulated S_{11}.

conversion loss is introduced and results are presented. The performance of the central diode and the dual offset diode structure are compared.

Finally, a fully quasi-optical simulation is presented, with plane-wave illumination of the structure simulated in the above sections, but with the microstrip line removed. The effective conversion-loss definition introduced in the previous section is then modified to account for plane-wave illumination. This conversion loss is then calculated over a wide frequency range to determine the optimum operating frequencies for these two particular structures. The diode position for the dual-diode structure is then optimized and, finally, the input plane-wave field strength is optimized for both central and offset diode structures. At the optimum frequencies, slot voltage distributions and radiation patterns at the fundamental and first harmonic frequencies are then presented for both central and offset diode structures and the effective conversion efficiencies of the structures are compared.

This paper shows how the LE-FDTD method can be used to analyze quasi-optical multiplying structures. Normally, this approach would be supplemented by an initial harmonic-balance optimization procedure using a circuit simulator in order to determine the optimum input impedance at the fundamental frequency and load impedances at the harmonic frequencies [12]. A slot antenna with the appropriate impedances could then be designed. Standard multiplier theory requires that the input and output circuits are isolated by frequency-selective networks to limit the interaction of the fundamental frequency signal in the load circuit and the harmonic signals at the input. However, in this highly integrated multiplier, no such filtering networks exist and, thus, this type of theory may not be directly applicable. Moreover, for the plane-wave-excited fully quasi-optical results, it is not clear that current circuit simulators could accurately model the plane-wave excitation. Thus, the LE-FDTD method can be seen as one of the key components in the design and analysis of the rapidly expanding field of quasi-optical circuits.

II. Passive Validation

In order to validate the method, a microstrip-fed single slot antenna was constructed and measured using in-house facilities. The method has been previously compared with analytic methods and good agreement has been obtained [13].

In this paper, the slot antenna is formed in the ground plane of the microstrip feeding line, the structure is shown in Fig. 1(a). The microstrip line extends over the slot by a quarter-wavelength at the slot resonant frequency producing a short circuit at the slot resulting in a good transition to the slot line. The feed is offset close to the 50-Ω impedance point of the slot [14] resulting in good input return loss.

The slot measures 15.1 $\times$ 0.4 mm^2 and is discretized with 24 cells along the slot and four cells across the slot. Variable meshing is used [15], [16] to obtain six cells across the microstrip feed line. The substrate has a dielectric constant of $\epsilon_r = 3.38$ and a height of 0.813 mm and is discretized with four cells. The overall substrate dimensions are 25.0 $\times$ 23.5 mm^2 and these dimensions are reproduced exactly within the FDTD simulation resulting in an overall grid size of 39 $\times$ 115 $\times$ 57. Perfectly matched layers [17] are used as absorbing boundaries. The structure is enclosed by a field integration box for the calculation of radiation patterns using a near-to-far field transform [18].

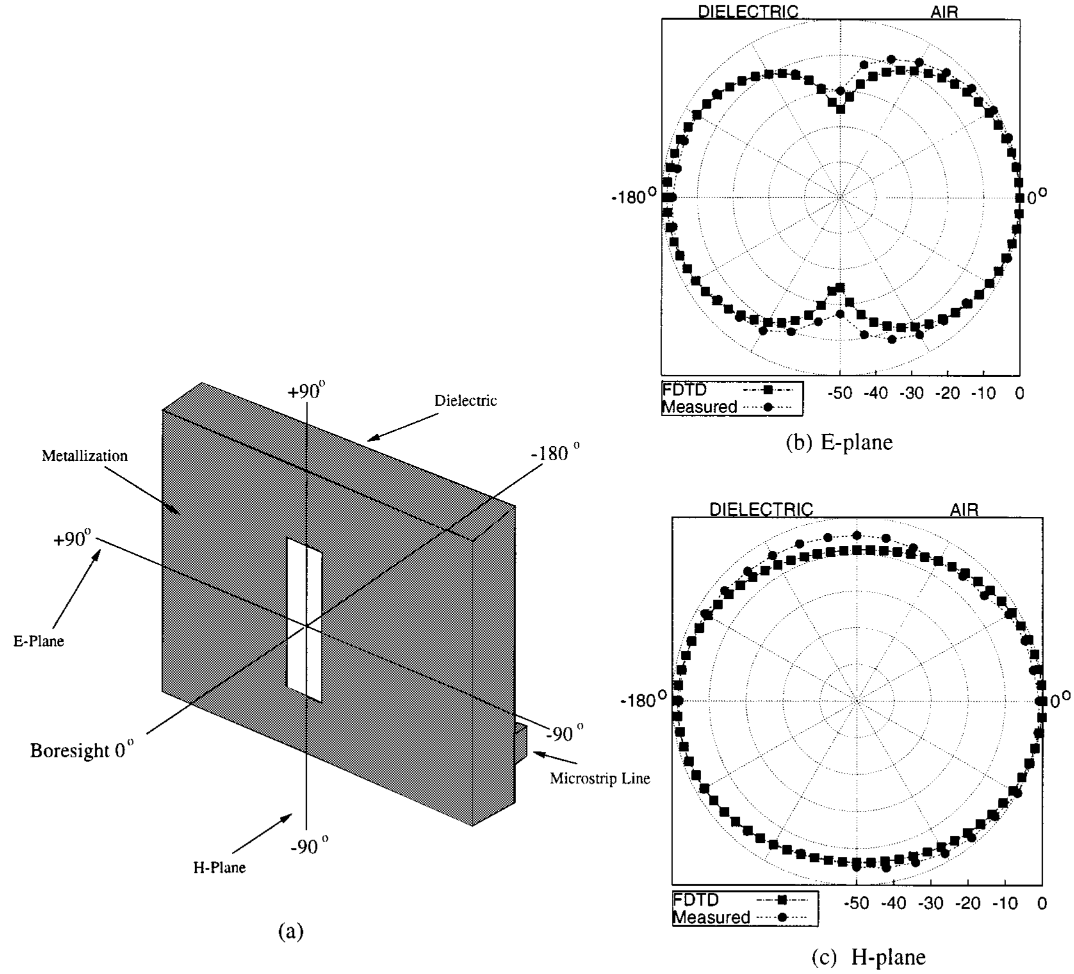


Fig. 2. (a) Radiation pattern definitions. (b)–(c) Radiation patterns for microstrip-fed passive slot antenna, measured −6.97 GHz and simulated −7.15 GHz.

The structure is excited with a Gaussian pulse from two lumped generators placed at the edges of the microstrip line in order to reduce the discontinuity caused by the lumped elements. A typical simulation takes 8 h on a Pentium II 333 MHz with 512 MB of RAM under a Linux OS. This results in complete S-parameter and radiation pattern data for any frequency up to 25 GHz. Without the radiation pattern calculation, the simulation time is reduced to 3.5 h. The voltage and current are calculated at the input to the microstrip line allowing the calculation of s_{11}. The results are shown in Fig. 1(b) and good agreement can be seen. The fundamental resonance of the antenna is seen to be near 7.0 GHz, and the first harmonic resonance is observed near 15.0 GHz.

The radiation patterns of the structure were then measured and simulated. The measurements were performed using a small anechoic chamber constructed using Eccosorb VHP-8 material. A PC-controlled rotating table allowed the measurements to be automated. The RF source was an HP 8720 vector network analyzer (VNA), and a Tektronix 492P spectrum analyzer was used as a receiver. The receiving antenna was either a length of WG12 waveguide for the 4–6-GHz band or WG16 for the 8–12-GHz band. Lengths of waveguide were used as receivers instead of horn antennas so as to minimize the far-field distance enabling this small chamber to give good results.

Fig. 2(a) shows the schematic of the structure with axes showing the angular definitions for the radiation patterns. Fig. 2(b) and (c) shows the measured and simulated radiation patterns (logarithmic scale) for the passive slot antenna. The overall structure of the patterns agree with the literature for slot antennas on finite substrates [19], i.e., omnidirectional in the H-plane and bidirectional with nulls at the metal surface in the E-plane. The agreement between the measured and simulated radiation patterns is good considering the connector and a feeding cable is also present only for the measured results.

III. Diode Model Validation

The key element to successfully modeling the quasi-optical multiplier is the diode model itself. The diode being used is a Hewlett–Packard HSMS-8202, dual in-series in a SOT-23 package. Ideally a single diode package would have been used, but these were not readily available to the authors. The model used for the diode has been obtained from an HP application note [20]. A detailed description of the LE-FDTD implementation of the large-signal diode model without parasitics is given in [3]. In this paper, the package parasitics are included and their values are tuned to match the measured performance of a diode mounted in series in a microstrip line. This procedure

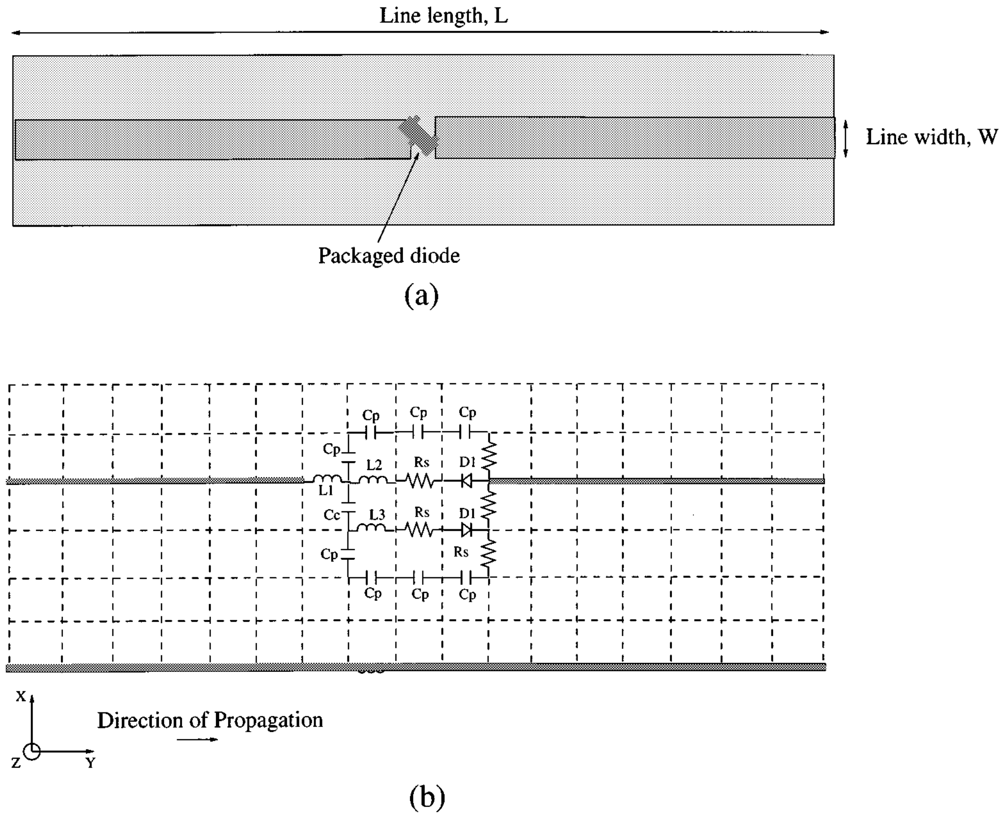


Fig. 3. (a) Schematic diagram of series diode measurement, $W = 1.88$ mm, $L = 12$ mm. (b) Schematic showing implementation of the diode model within the FDTD grid $D1 = I_s = 4.6e-8$, $C_{j0} = 0.18$ pF, $N = 1.09$, $V_j = 0.5$ V, $M = 0.5$, $FC = 0.5$, $C_p = 0.13$ pF, $C_c = 0.06$ pF, $R_s = 6\ \Omega$, $L_1 = 0.05$ nH, $L_2 = L_3 = 0.8$ nH, $dx = 0.2032$ mm, $dy = 0.1$ mm, $dz = 0.313333$ mm and $dt = 0.287$ ps.

is required since it has been found that the lumped elements exhibit nonideal behavior against frequency, which it seems is caused by the discretization of the FDTD grid.

The microstrip line was constructed on a substrate with dielectric constant of $\epsilon_r = 3.38$ and height 0.81 mm. A 50-Ω linewidth of 1.88 mm and a line length of 12 mm were used in both measurement and simulation. A schematic of the diode mounted on the line is shown in Fig. 3(a). In the FDTD implementation, the line is discretized with six cells across the line and four cells in the height of the dielectric. The grid is uniform in both of the x-, and z-directions, with a grid size of $\Delta x = 0.20$ mm in the height of the dielectric and $\Delta z = 0.31$ mm across the line. In the y-direction, variable meshing is used in order to replicate exactly the mesh in which the diode will be placed for the slot antenna simulations. This is of utmost importance since, in this way, the nonideal behavior will be exactly replicated in the slot antenna simulations. Thus, $\Delta y = 0.1$ mm is used across the region of the diode model.

When a nonlinear device such as a diode is added to the structure, a simple Gaussian pulse excitation can no longer be used since this introduces a dc level. Thus, a Gaussian modulated sine wave was used. The pulse has a peak value of 0.01 V, which is equivalent to -36 dBm from a 50-Ω source into 50-Ω load. This input power maintains the diode in the small-signal regime. A section through the LE-FDTD grid is shown in Fig. 3(b). The intrinsic diode $D1$ has the following SPICE parameters: saturation current $I_s = 4.6 \times 10^{-8}$ A, zero-bias junction capacitance $C_{J0} = 0.18$ pF, emission coefficient $N = 1.09$, junction potential $V_J = 0.5$ V, grading coefficient $M = 0.5$, and coefficient for forward bias depletion capacitance $FC = 0.5$. The parasitic model elements are the package capacitance $C_p = 0.13$ pF, coupling capacitance $C_c = 0.06$ pF, series resistance $R_s = 6\ \Omega$, bond-wire inductance $L_1 = 0.8$ nH, and lead frame inductance $L_2 = 0.05$ nH.

The final modeled and measured S-parameters are shown in Fig. 4. Reasonably good agreement is observed. Good agreement of the frequency of the first resonant is seen. These results show the LE-FDTD can model the performance of a packaged Schottky diode quite well and, thus, the model can be used to evaluate the performance of a diode multiplier.

IV. Small-Signal Results

The packaged diode model was then added to the structure of Section II. A Gaussian modulated sine wave was again used. The maximum amplitude of the pulse was again 0.01 V. The small-signal results are a useful validation of the diode model with nonlinear effects removed.

As mentioned in Section I, the diode is unbiased to reduce the complexity of the circuit since it is being designed for array applications. The diode was added to the center of the slot and small-signal S-parameters and radiation patterns were simulated and measured. These are shown in Fig. 5. The input return loss shows very good agreement [see Fig. 5(a)]. The fundamental resonance is now shifted down in frequency to 4.65 GHz due to the loading of the diode. The second resonance remains unchanged,

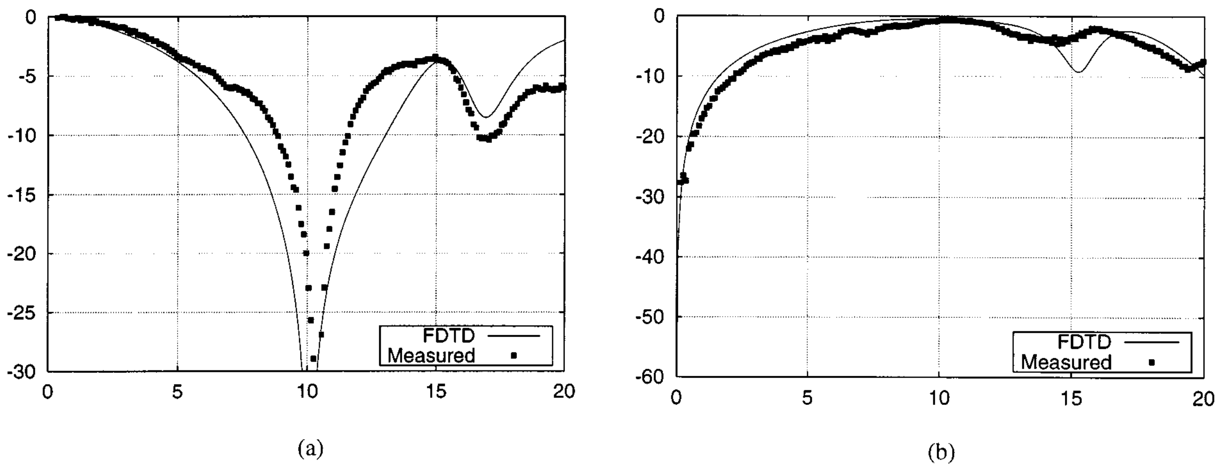


Fig. 4. Measured and simulated small-signal S-parameters of a HSMS-8202 diode mounted in series in a 50-Ω line. (a) S_{11}. (b) S_{21}.

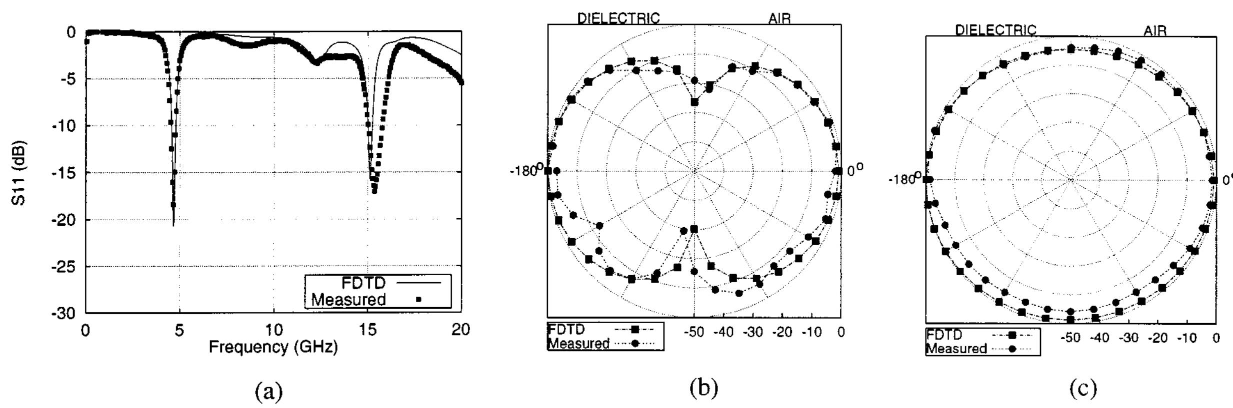


Fig. 5. Central-mounted diode measured and simulated small-signal results. (a) S_{11}. (b) E-plane measured and simulated at 4.65 GHz. (c) H-plane measured and simulated at 4.65 GHz.

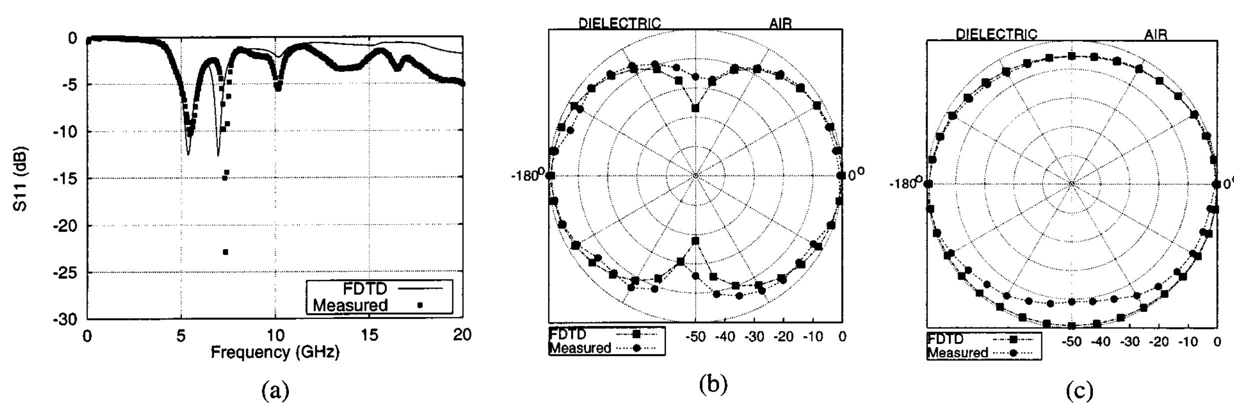


Fig. 6. Dual-offset diode measured and simulated results. (a) S_{11}. (b) E-plane measured and simulated -5.35 GHz. (c) H-plane measured and simulated -5.35 GHz.

as might be expected, since this will have a zero voltage at the center of the slot. The radiation patterns [see Fig. 5(b) and (c)] also show reasonably good agreement apart from a null at -150° in the E-plane [see Fig. 5(b)], which the authors feel is due to scattering from the antenna rotating structure.

To investigate possible optimization of the structure, the central diode was replaced with two offset diodes placed at either end of the slot. The impedance at the end of the slot is found to be lower than at the center and could be more suited to matching Schottky barrier diodes used in quasi-optical multipliers. The diodes were positioned at 2.13 mm from the ends of the slot. The simulated and measured results are shown in Fig. 6. The input return loss now shows two low-frequency resonances [see Fig. 6(a)]. The fundamental mode is now measured to be at 5.45 GHz, higher than when the diode is in the center due to the reduced loading because of the offset diodes. The first harmonic

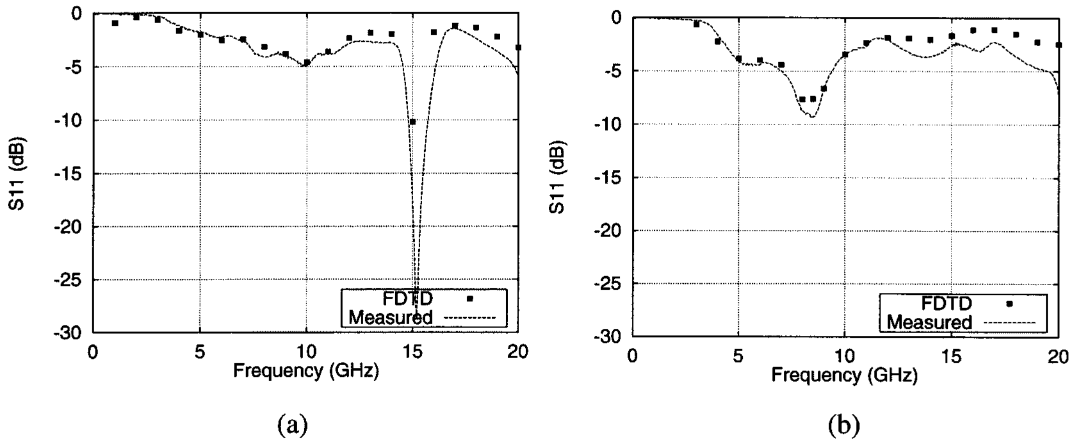


Fig. 7. Measured and simulated large-signal S_{11}. (a) Central-mounted diode. (b) Dual-offset diode.

resonance is no longer observed and is probably damped by the diode position. The higher frequency resonance, simulated at 6.95 GHz, appears to be a spurious radiating mode strongly dependent on diode position possibly induced by self-resonance within the diode package. The radiation patterns [see Fig. 6(b) and (c)] are again similar to the passive case and show good agreement between measurement and simulation.

In Figs. 6(a) and 7, it is noted that the agreement between measured and simulated return loss becomes less good at higher frequencies. This is the result of two main factors. Firstly, FDTD has an inherent frequency-dependent error (dispersion) due to the discretization. This error can be kept low by maintaining grid cell sizes less than one-tenth of a wavelength. Secondly, the accuracy of the lumped-element diode model will tend to become worse at higher frequencies. Not only is this due to the normal limitations of lumped-element models, but here there is also the fact that the model is embedded within the FDTD grid and this leads to further dispersion effects associated with the LE-FDTD method.

V. Large-Signal Results

In order to investigate multiplier operation, it is necessary to operate under large-signal conditions; the nonlinearity of the junction resistance will then cause multiplying to occur. It is necessary to excite the structure with pure sinusoids since multiple frequency excitation will produce many mixing products making the performance difficult to determine. The input voltage amplitude is now 2.0 V, this is equivalent to $+10$ dBm into a 50-Ω load. The large-signal S-parameter results for the center mounted diode are shown in Fig. 7(a). The large-signal scattering parameters have been measured by increasing the HP8720 output power to $+10$ dBm. The simulation points are obtained by running sinusoidal simulations at each individual frequency point. As can be seen, very good agreement is obtained. The low-frequency resonance is no longer present, most probably because the diode will be strongly forward biased by the large-signal input and the diode resistance will be quite low and is "shorting out" the slot resonance. Fig. 7(b) shows the performance of the slot antenna with offset diodes.

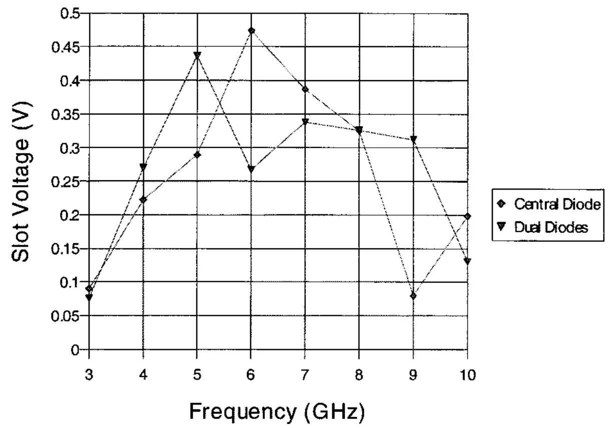
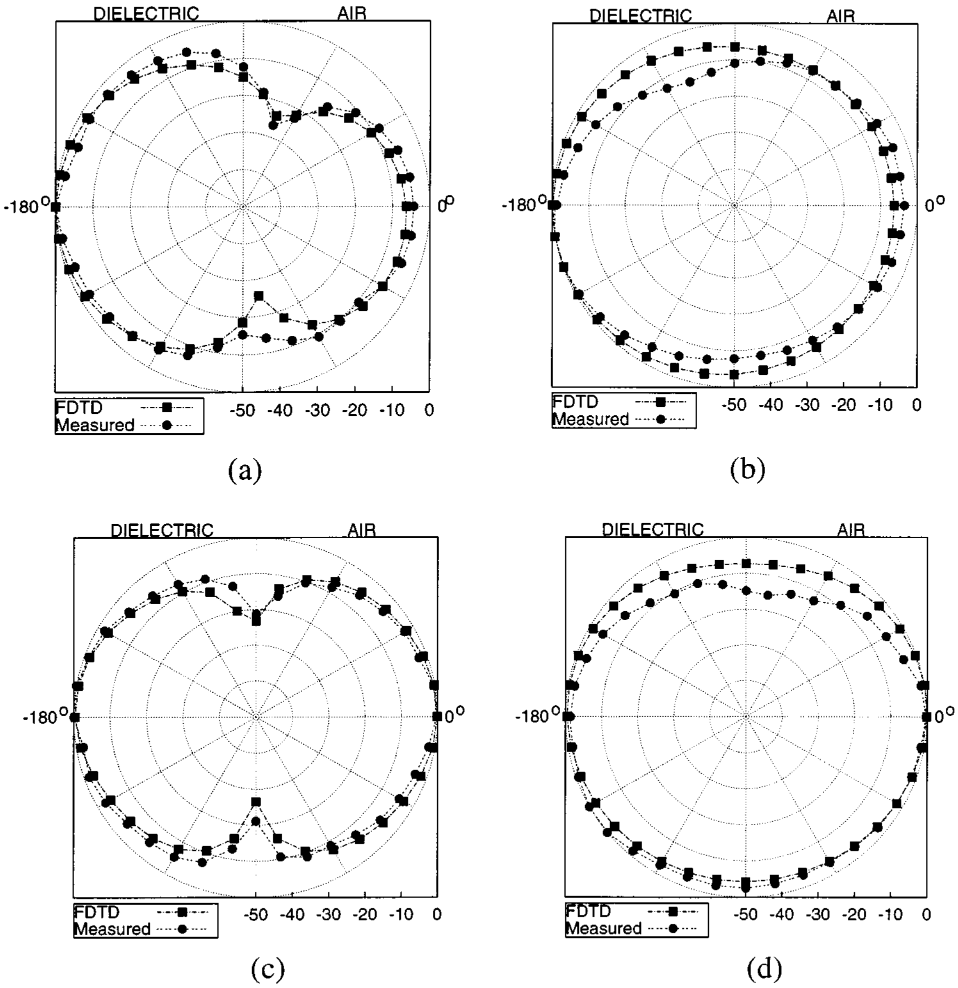


Fig. 8. First harmonic slot voltage for central- and dual-offset diodes.

Again, good agreement is observed. It is seen that reasonable input return loss of 9 dB is maintained at 8.5 GHz. This should be the result of both less loading of the slot by the diodes and that the low forward-bias diode resistance matches the slot impedance more closely near the end of the slot.

In order to determine the optimum large-signal operating frequency, the first harmonic slot voltage has been used as a guide to conversion efficiency. Ideally, the first harmonic far-field power density should be used. However, this requires large amounts of computing time and memory and, as might be expected, from antenna theory [19], the maximum far-field electric-field strength is directly proportional to the maximum slot voltage in the case of a uniform voltage distribution. Thus, in this case, where we are interested in comparing measured and simulated performance and not in determining the optimum, the slot voltage is sufficient to indicate a frequency that will be close to that of maximum conversion efficiency. The voltage is calculated by taking a line integral across the slot in each cell along the slot. This then is Fourier transformed at the first harmonic frequency giving the voltage distribution in the slot. These distributions can be evaluated at a number of frequencies across the operating bandwidth of the multiplier and the maximum value determined to give the optimum operating frequency. The results are shown in Fig. 8. An optimum



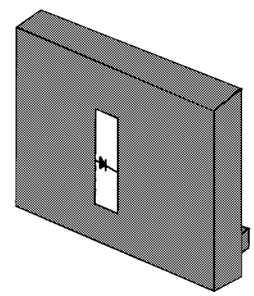


Fig. 9. Measured and simulated large-signal radiation patterns for central-mounted diode at 6 and 12 GHz. (a) Fundamental E-plane. (b) Fundamental H-plane. (c) First harmonic E-plane. (d) First harmonic H-plane.

frequency of 6 GHz is found for the central diode and 5 GHz for the offset diodes.

The radiation patterns for the center mounted diodes are shown in Fig. 9. Fig. 9(a) and (b) shows the fundamental frequency patterns at 6 GHz. It is noted that the patterns are now biased toward the dielectric side by 5–6 dB, and this effect is predicted reasonably well by the LE-FDTD method. Fig. 9(c) and (d) shows the first harmonic patterns at 12 GHz and, again, reasonably good agreement is observed.

The radiation patterns for the dual-offset diodes are shown in Fig. 10. Fig. 10(a) and (b) shows the fundamental frequency patterns at 5 GHz. Fig. 10(c) and (d) shows the first harmonic patterns at 10 GHz. All patterns show reasonably good agreement.

Having observed the first harmonic patterns, it is important to discuss the absolute power level of the first harmonic relative the fundamental since this will define the conversion loss. In the case of the microstrip-fed structures, the input power is well defined as +10 dBm. However, the output is in free space. From FDTD, we obtain a field strength at a particular distance, and from measurement, we obtain power received by a horn antenna at a particular distance. We can relate the two using the Friis formula [19], which relates received to transmitted power in a antenna system

$$P_r = G_t G_r \left(\frac{\lambda}{4\pi r}\right)^2 P_t. \tag{1}$$

Fig. 11 describes the quantities in the Friis formula. P_r is the received power, P_t is the transmitted power, G_r is the receiver gain, G_t is the transmitter gain, λ is the free-space wavelength, and r is the distance between the transmitter and receiver. For the measured results, we define P_t as the power transmitted by the slot antenna at the first harmonic frequency and G_t as the gain of the slot antenna at the first harmonic frequency. Thus, in order to calculate the power radiated at the first harmonic, we need to know the gain of the active slot antenna at the first harmonic. This is not an easy task since the slot is loaded with diode, thus the concept of effective isotropic radiated power (EIRP, P_{eir}) has been introduced [1]. The EIRP is defined as the product of P_t and G_t, thus, it is the power that would have to be radiated by an isotropic antenna in order to produce the same received power. Thus, to measure EIRP, neither P_t or G_t is required to be known, only the product, which can be easily

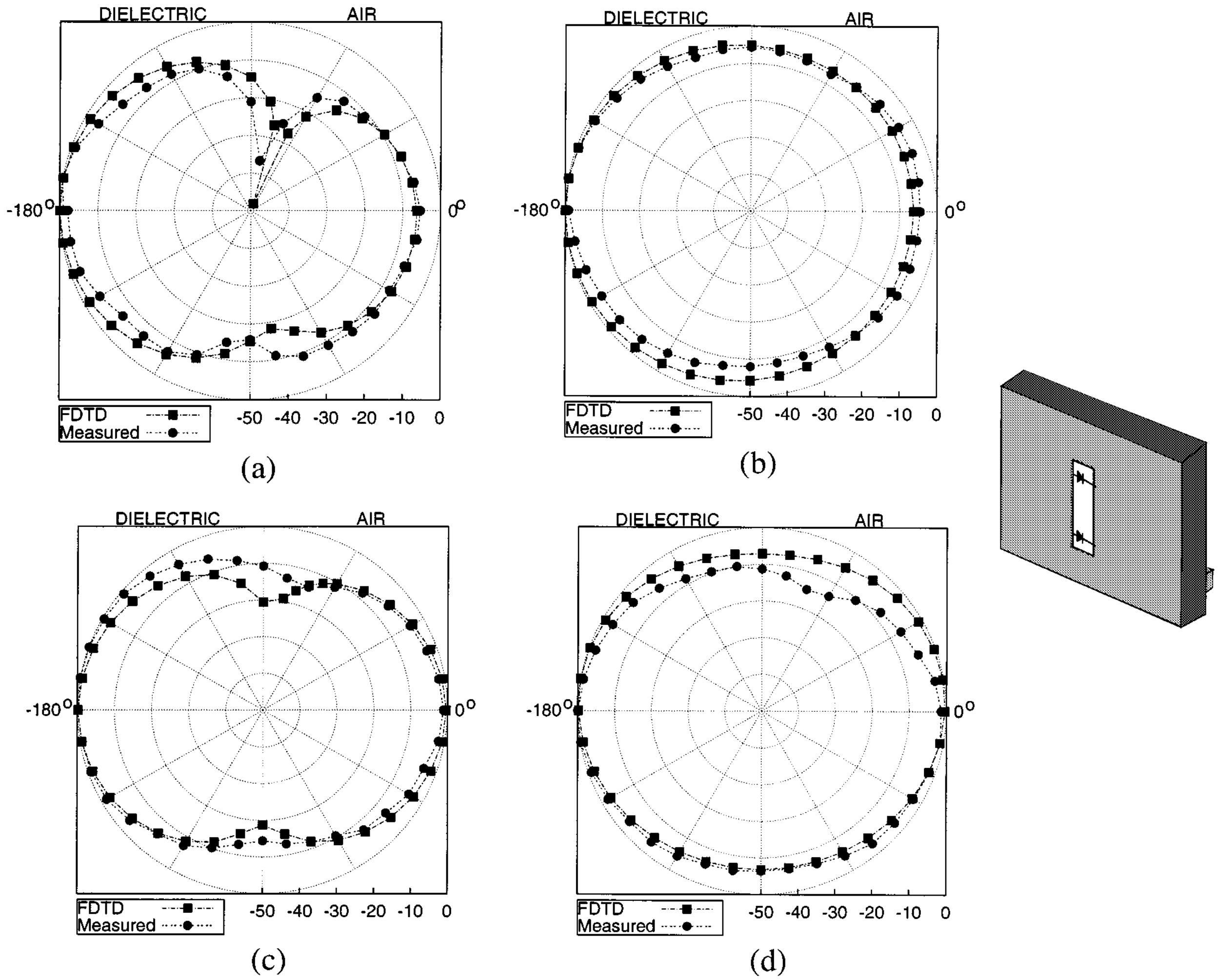


Fig. 10. Measured and simulated large-signal radiation patterns for dual offset diodes at 5 and 10 GHz. (a) Fundamental E-plane. (b) Fundamental H-plane. (c) First harmonic E-plane. (d) First harmonic H-plane.

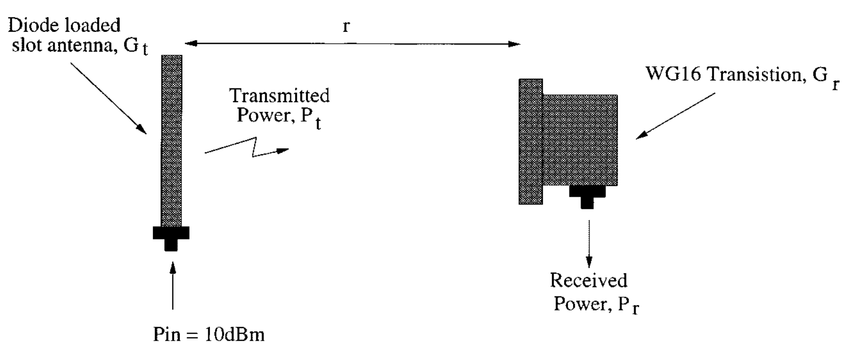


Fig. 11. Schematic diagram showing measurement of received power from the diode loaded slot antenna.

deduced from the Friis formula. Thus, in this paper, we will use this measure to compare the performances of antennas and to produce a quantity defined as effective conversion loss. The effective conversion loss L_{ec} is defined as

$$L_{\text{ec}} = \frac{P_{\text{in}}^{f_0}}{P_t^{f_1} G_t^{f_1}} \tag{2}$$

which is the ratio of input power at the fundamental frequency f_0 to the EIRP at the first harmonic frequency f_1. In order to calculate the EIRP from the FDTD field strength data, we can use the relationship between the EIRP and power density S

$$P_{\text{eir}} = 4\pi r^2 S. \tag{3}$$

S being related to the field amplitude by $S = |E|^2/\eta_0$ with $\eta_0 = 120\pi$ for free space. Equation (3) shows that, for an isotropic radiator, the total power radiated is simply the power density at a particular distance r multiplied by the area of the sphere, radius r, enclosing the radiator.

TABLE I
MEASURED AND SIMULATED EFFECTIVE CONVERSION LOSS

	Measured			FDTD		
	Received Power [dBm]	EIRP [dBm]	L_{ec} [dB]	Simulated E-field [V/m]	EIRP [dBm]	L_{ec} [dB]
Central diode	-38.29	-2.18	12.18	0.1173	0.14	9.86
Dual diodes	-42.19	-6.33	16.33	0.0816	-3.01	13.01

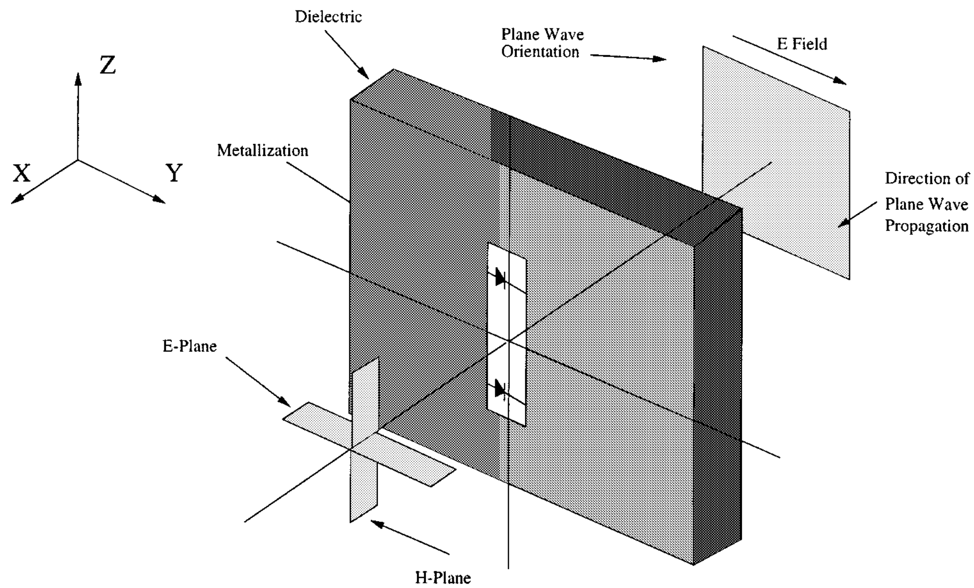


Fig. 12. Schematic diagram of quasi-optical simulation of diode slot multiplier, showing plane-wave orientation.

We can now calculate the measured and simulated effective conversion losses. Fig. 11 shows the measurement setup. The radiated power is measured from the slot antenna at the first harmonic frequency at a distance of 266 mm using a WG16 transition as a horn antenna. Table I shows the results. The measured received power results show that more power is obtained in the central-diode case, which agrees with the slot voltage results of Fig. 8, thus confirming their validity. The EIRP is approximately 36 dB greater than the received power, which is made up of the free-space loss and the gain of the WG16 transition. From the EIRP, the effective conversion loss is calculated, the central diode has a figure of 12.2 dB, about 4 dB higher than the dual-diode case. The simulated results show an effective conversion loss of 9.9 dB for the central diode and 13 dB for the dual diode. While these are somewhat different in absolute level from the measured results, they show a similar factor of improvement for the central diode over the dual diode, which is about 3 dB simulated and 4 dB measured. The differences in absolute level can be accounted for by three main factors. Firstly, here, FDTD assumes lossless conductors and dielectrics, resulting in better simulated conversion losses than measured. Secondly, the diode model being used does not include variable series resistance and reverse breakdown effects, again improving the simulated results. Thirdly, the experimental results are quite difficult to obtain, and any misalignment between the slot multiplier and the receiving horn will increase the measured conversion loss. Overall, however, the behavior is predicted reasonably well.

From these results, it would seem that the central-diode configuration is better than dual diode. However, it must be remembered that these structures have not been optimized, either for input and output impedances seen by the diode or input power level, an important parameter when a zero bias design is being used. Thus, a definitive statement as to the best structure cannot be made without further investigation.

This section has shown that the LE-FDTD method can predict reasonably well the performance of quasi-optical circuits, in terms of large-signal input impedance, radiation patterns, and nonlinear parameters such as conversion loss. This would allow this type of circuit to be optimized to achieve minimum conversion loss. A number of parameters could be investigated, including substrate height, important for the suppression of surface wave modes [6], input power level, slot width, and for the dual-diode case, diode position. In the following section, simulated results for structure optimization are shown for the fully quasi-optical case with plane-wave input and radiated output.

VI. PLANE-WAVE RESULTS

Having looked at microstrip-fed quasi-optical circuits, we can now use the LE-FDTD method to investigate the performance of plane-wave excited structures. Fig. 12 shows a schematic of the plane-wave simulation. The slot antenna has the same dimensions as that of Fig. 1 with the microstrip line removed. However, in order to prevent diffraction from ground plane edges

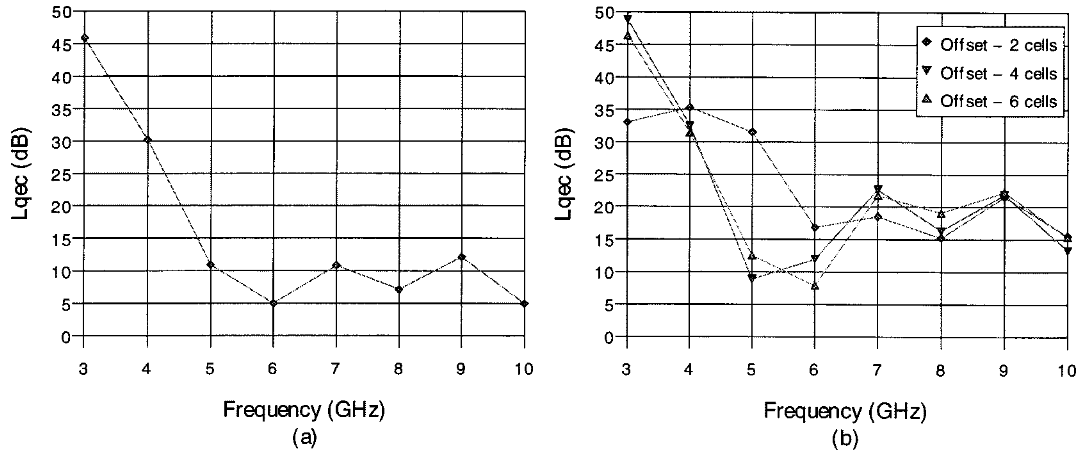


Fig. 13. Quasi-optical effective conversion loss $L_{\rm qec}$ as a function of frequency with input field strength of 100 V/m for: (a) central-mounted diode and (b) dual-offset diodes.

the E-plane, substrate dimension has to be less than $\lambda/2$ at the highest frequency [19]. Thus, the length of the substrate has been reduced from 25 to 8.8 mm, allowing operation up to 17 GHz. The structure is excited with a plane wave at the fundamental frequency and power is scattered by the structure at both the fundamental and first harmonic frequencies. As well as a radiation integration box, which is used in the near- to far-field transformation, a second box is now required for plane-wave excitation. The total-field/scattered-field formulation [21] is used, and this requires the region of total fields to be defined. A plane wave with a field strength of 100 V/m is incident on the structure, this delivers approximately $+5$ dBm to the slot antenna.

A different definition of effective conversion loss is required here since the input is defined in terms of field strength or power density. In a similar way to the coaxial fed results, we can take the ratio of input power density S_i to EIRP $P_{\rm eir}$, this quantity is denoted $L'_{\rm ec}$

$$L'_{\rm ec} = \frac{S_i}{P_{\rm eir}}. \tag{4}$$

If this quantity is inverted, it has units of area and can be thought of as an effective area for the antenna A_e. Using (3) to express $P_{\rm eir}$ in terms of power density, we obtain

$$A_e = S_o \frac{4\pi r^2}{S_i} \tag{5}$$

where S_o is the output power density at the doubled frequency. Using the well-known relationship between effective aperture and the gain of an antenna [19] and expressing the power densities in terms of field strengths, we can thus obtain an effective quasi-optical conversion gain for the antenna $G_{\rm qec}$

$$G_{\rm qec} = \frac{|E_o|^2}{|E_i|^2} \left(\frac{4\pi r}{\lambda}\right)^2 \tag{6}$$

and, thus, effective quasi-optical conversion loss is $L_{\rm qec} = 1/G_{\rm qec}$. In the expression above, $|E_i|$ is the input plane-wave field strength at the fundamental frequency, $|E_o|$ is the maximum field strength at the first harmonic frequency, λ is the free-space wavelength at the first harmonic frequency, and r is the distance from the antenna to the far-field point where $|E_o|$ is sampled. The quantity $L_{\rm qec}$ is seen to be simply the ratio of the square of the input and output field strengths multiplied by the free-space loss from the antenna to the point where the field is sampled, which will be used as a figure-of-merit to compare the following simulated results.

In order to find the optimum conversion-loss frequency, sinusoidal simulations have been performed at frequencies from 3 to 10 GHz in 1-GHz steps. The results for both single- and dual-diode structures are shown in Fig. 13(a) and (b), respectively. In the dual-diode case, a number of different diode positions have been investigated. The results for the central diode show a minimum effective conversion loss of 5 dB at 6 and 10 GHz. This seems an unrealistically low figure, but it has to be remembered this is an effective conversion loss, which includes the focusing effect of the slot antenna, both at the input and output. These figures are useful for comparing different simulated structures. Fig. 13(b) shows the results for the dual-diode case for three different diode positions two cells (1.1 mm), four cells (2.47 mm), and six cells (3.83 mm) from the ends of the slot. It is seen that the minimum effective conversion loss is obtained at six cells from the end of the slots and at 6 GHz. The minimum value is 7.9 dB somewhat higher than for the single diode structure as in the microstrip-fed case shown above.

As mentioned previously, this is a zero-biased design in order to reduce the overall circuit complexity. Thus, the input power produces a self-biasing effect in the diode and, thus, the input power level is a critical parameter in this design. Simulations have, therefore, been performed at different power levels in an attempt to obtain optimum performance. Fig. 14 shows the results of the simulations for the central-diode case and the six cell offset diode case. The simulations have been performed at 50 V/m, a lower power level, two higher power levels (200 and 400 V/m). Fig. 14(a) shows the central-diode case and it is seen that best performance is obtained at an input field strength of 200 V/m and at 8.0 GHz with $L_{\rm qec} = 4.47$ dB. Fig. 14(b) shows the offset diode case with diodes six cells from the end of the slot and it is seen that best performance is again obtained at an input field strength of 200 V/m at 6.0 GHz with $L_{\rm qec} = 5.36$ dB.

These are examples of the type of optimization that could be performed using the LE-FDTD method. One of the main limitations, however, is computing time, with each frequency point

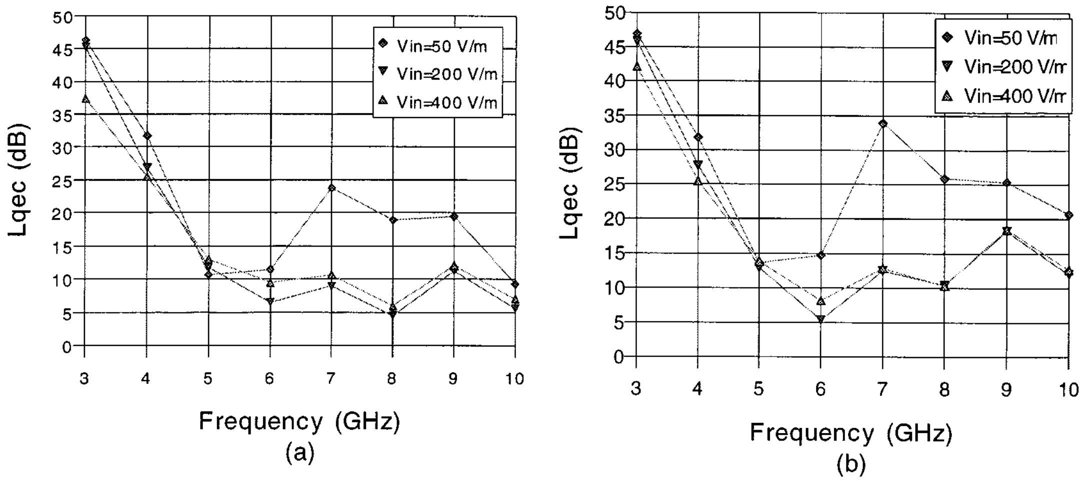


Fig. 14. Quasi-optical effective conversion loss $L_{\rm qec}$ as a function of frequency and input field strength for: (a) central-mounted diode and (b) dual-offset diodes.

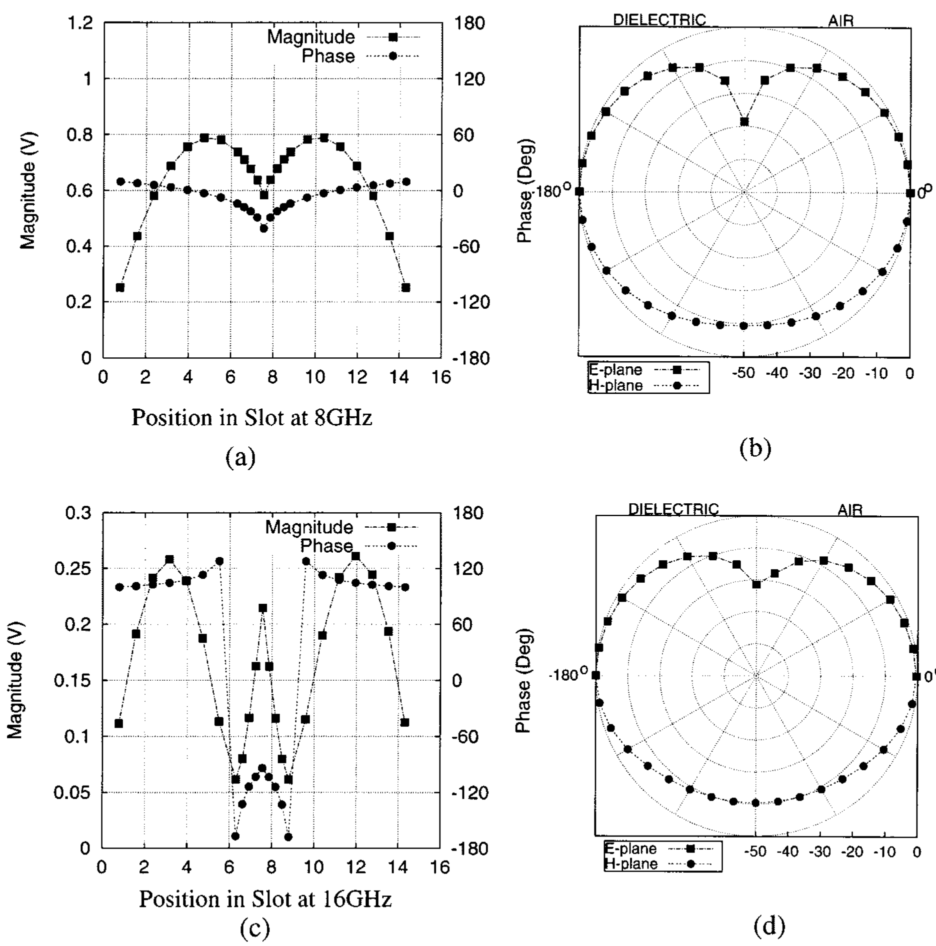


Fig. 15. (a), (c) Voltage distributions and (b), (d) radiation patterns with sinusoidal plane-wave excitation for a single slot antenna with a central diode at the fundamental resonant frequency (8 GHz) and its first harmonic (16 GHz) with input field strength of 200 V/m.

taking approximately 8 h of CPU time on a Pentium II 333 MHz with 512 MB of RAM under Linux OS. However, with ever increasing processor speed in the near future, structure optimization using the LE-FDTD method may be feasible.

The radiation pattern results can now be shown for the two structures at the two optimum frequencies. As well as radiation patterns, another useful type of result can be obtained from the FDTD method by taking the line integral of the E-field across the slot at each cell position along the slot. The Fourier transform of this then gives the voltage distribution, in both magnitude and phase, along the slot at a particular frequency. This has been found useful for understanding the behavior of the slot antenna. Fig. 15 shows the voltage distributions and field patterns for the central-diode case with 200-V/m input

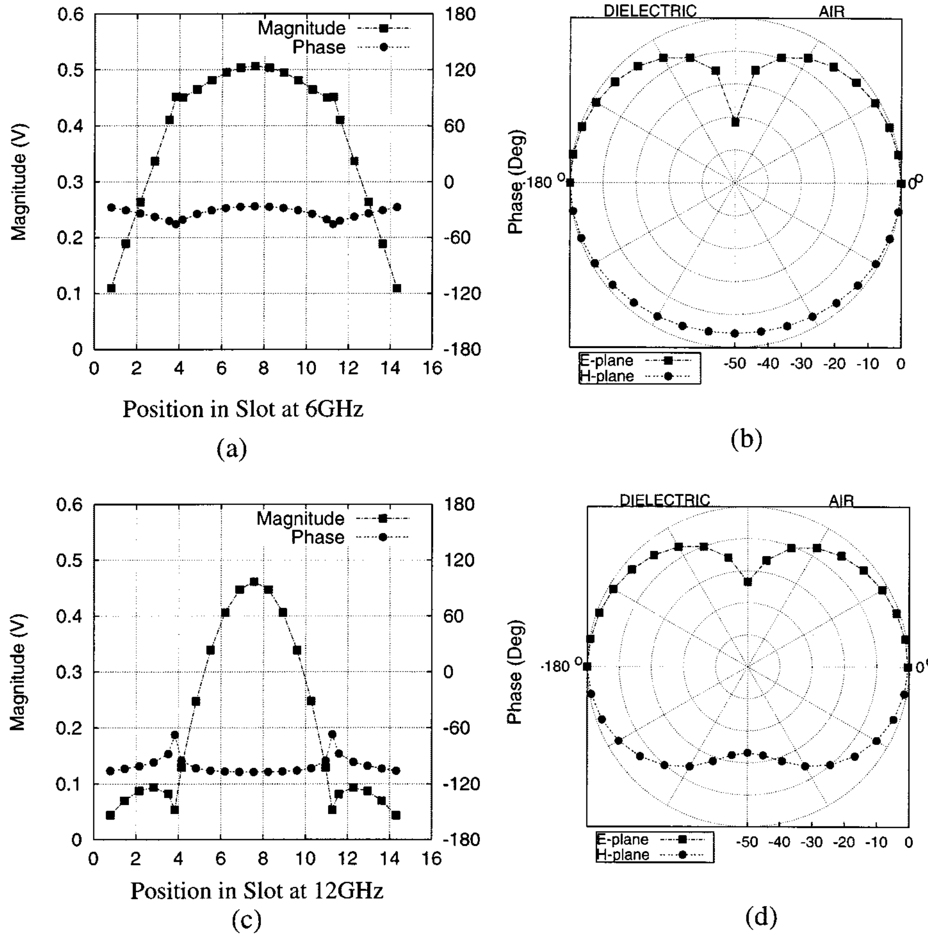


Fig. 16. (a), (c) Voltage distributions and (b), (d) radiation patterns with sinusoidal plane-wave excitation for a single-slot antenna with two offset diodes at the fundamental resonant frequency (6 GHz) and its first harmonic (12 GHz) with input field strength of 200 V/m.

field strength. Fig. 15(a) shows the fundamental frequency voltage distribution at 8 GHz and, as might be expected, it is basically half-sinusoidal with a discontinuity at the diode position. The phase is seen to be relatively constant across the slot. The fundamental frequency patterns are shown in Fig. 15(b), unlike the microstrip-fed case, they are now symmetrical since the structure is also symmetrical, thus only half the patterns are shown. They are again similar to the passive slot antenna patterns. This is mainly due to the correct choice of ground-plane dimension, with larger ground planes, lobes due to diffraction from ground plane edges can form. Fig. 15(c) shows the first harmonic voltage distribution at 16 GHz and, as might be expected, a double sinusoid distribution is observed with a large discontinuity at the diode. The phase associated with each half-sinusoid is approximately equal, as expected, for a one-wavelength-long slot antenna excited by a even mode, an example of which is a plane wave [19]. If the excitation is odd mode or unsymmetrical, then antiphase phase distributions are observed.

Fig. 16 shows the voltage distributions and radiation patterns for the dual-diode case with six cell offset and 200-V/m input field strength. The fundamental voltage distribution in Fig. 16(a) is again basically half sinusoidal with discontinuities at the diodes and the radiation patterns are similar to the central-diode case. The first harmonic voltage distribution in Fig. 16(c) is now no longer double sinusoidal since the position of the diodes do not allow this mode to exist. Fig. 16(d) shows the first harmonic radiation patterns they are again similar to the passive case, and it can be seen that the gain is higher in the first harmonic case, as in case of a full-wave dipole [19].

Thus, we have seen that LE-FDTD method can be used to analyze and optimize fully quasi-optical structures. An effective quasi-optical conversion loss has been defined and used to compare the different structures. Diode position has been used as a new design parameter by using a dual-diode structure. The dual-diode structure shows a conversion loss 0.89 dB worse than for a central-diode structure.

VII. Conclusions

This paper has presented a detailed validation of the LE-FDTD method using a quasi-optical slot multiplier as an example circuit. Firstly, results for a passive structure were presented, then a diode model was validated and added to the slot antenna. Both small- and large-signal results were then presented showing that LE-FDTD method can predict with a reasonable degree of accuracy the performance of this type of quasi-optical circuit. Finally, a fully quasi-optical multiplier was simulated and both structure and input power level optimizations were performed, highlighting the power of this approach to produce optimally designed quasi-optical circuits. Some important points should be noted. Firstly, this is only a single-slot antenna, these circuits are envisaged in large arrays. To simulate a whole array would be unfeasible. However, by using Floquet boundary conditions and a unit cell approach, it should be possible to produce results for infinite arrays. Secondly, the effect of the diode package itself on the radiation is not currently being accounted for since the package consists of a plastic case that is placed in the radiating slot. By obtaining the dielectric constant of the package, a dielectric block could be included to give further improvements in accuracy.

The final goal of this paper is to optimize millimeter and sub-millimeter wave multipliers. In order to carry out simulations at these frequencies, two important issues must be addressed. Firstly, metal and dielectric losses will be significant and must be included in the simulations. The problem of frequency-dependent loss across the large bandwidth from f_o to $2f_o$ must also be addressed. The second issue is that of the diode model. At 300 GHz, a number of new effects are observed such as current saturation and electron inertia [22], and these will have to accounted for by using a more complex diode model. Measurements of the diode will have to be carried out in both small- and large-signal regimes so that a good diode model can be extracted.

We have shown that the LE-FDTD method is one of the few methods capable of simulating the entire problem of quasi-optical circuit analysis in a truly concurrent way. The LE-FDTD method is thus an important tool for the design and analysis of quasi-optical circuits, which are becoming very popular due to their high levels of integration and multifunctionality.

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S. Helbing, photograph and biography not available at time of publication.

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